AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0033] as follows:

[0033] The operation of the circuit 200 is now described with respect to FIGS. [[3]] 2 and 5. In a normal mode of operation, the differential amplifier 204 is enabled (i.e., the enable signal ENABLE has a value that enables the amplifier 204), the reference voltage Vref is the specified reference voltage (i.e., not grounded or floated) and the first inverter 206 is disabled (i.e., the self-refresh enabled signal SELF_REFRESH_ENABLED has a value that disables the inverter 206). This means, that the first inverter 206 has a logic low TTL* signal. With this setup, the differential amplifier 204 is used to sense when the SDRAM should be placed into the low power mode (i.e., when the clock enable signal CKE is driven to a low logic level).

Please amend paragraphs [0060]-[0062] as follows:

[0060] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908 which include at least one memory device 100 of the present invention. The memory components 908 may be a memory card or a memory module. Examples of memory modules include single inline memory modules (SIMMs) and dual inline memory modules (DIMMs). The memory components 908 may include one or more additional devices 909. For example, in a SIMM or DIMM, the additional device 909 might be a configuration memory, such as a serial presence detect (SPD) memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively, other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 ~~include~~ includes peripherals or controllers which are bus masters or which support direct memory access (DMA), the

memory controller 902 may implement a cache coherency protocol. If the memory controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0061] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, ~~an~~ a miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and ~~an~~ a legacy device interface 920. The primary bus bridge 903 may also coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0062] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be an local area network interface, such as an Ethernet card. The secondary bus bridge 916 may be used to interface additional devices via another bus to the processing system 900. For example, the secondary bus bridge 916 may be ~~an~~ a universal serial port (USB) controller used to couple USB devices 917 ~~via~~ to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to ~~one~~ additional devices such as speakers 919. The legacy device interface 920 is used to couple legacy devices 921, for example, older styled keyboards and mice, to the processing system 900.